

What is claimed is:

1. A delay locked loop device comprising:

5 a first delay line for receiving an external clock signal and a first delay control signal to generate a first internal clock signal;

a second delay line for receiving the external clock signal and a second delay control signal or the first delay control signal to generate a second internal clock signal;

10 a first delay control block for receiving the external clock signal to generate the first delay control signal;

a second delay control block for receiving the external clock signal to generate the second delay control signal; and

15 a phase detecting block for receiving the first internal clock signal and the second internal clock signal to generate the on-off signal by comparing a phase of the first internal clock signal with a phase of the second internal clock signal.

2. The delay locked loop device as recited in claim 1,  
20 wherein the second delay control block is disabled in response to the on-off signal when the delay locked loop device is locked.

3. The delay locked loop device as recited in claim 1,  
25 wherein the phase detecting block generates a weight signal in response to the first internal clock signal and the second internal clock signal.

4. The delay locked loop device as recited in claim 3,  
wherein the first delay control block generates a first duty  
controlled internal clock signal in response to the first  
internal clock signal, the second internal clock signal and  
5 the weight signal.

5. The delay locked loop device as recited in claim 4,  
wherein the second delay control block generates a second duty  
controlled internal clock signal in response to the first  
10 internal clock signal, the second internal clock signal and  
the weight signal.

6. The delay locked loop device as recited in claim 1,  
wherein the second delay line includes a second delay line  
15 control unit for receiving the first delay control signal or  
the second delay control signal to generate a first delay line  
enable signal and a delay line up-down signal as the first  
delay control signal.

20 7. The delay locked loop device as recited in claim 6,  
wherein the second delay line includes:

a coarse delay line in response to the first delay line  
enable signal and the delay line up-down signal for coarsely  
delaying the external clock signal; and

25 a fine delay line in response to the first delay line  
enable signal and the delay line up-down signal for finely  
delaying the coarsely delayed external clock signal to

generate the first internal clock signal.

8. The delay locked loop device as recited in claim 1,  
wherein the first delay line includes a first delay line  
5 control unit for receiving the first delay control signal to  
generate a first delay line enable signal and a delay line up-  
down signal as the first delay control signal and to provide  
the first delay control signal to the second delay line  
instead of the second delay control signal when the delay  
10 locked loop device is locked.

9. The delay locked loop device as recited in claim 8,  
wherein the first delay line includes:

a coarse delay line in response to the first delay line  
15 enable signal and the delay line up-down signal for coarsely  
delaying the external clock signal; and

a fine delay line in response to the first delay line  
enable signal and the delay line up-down signal for finely  
delaying the coarsely delayed external clock signal to  
20 generate the first internal clock signal.

10. The delay locked loop device as recited in claim 5,  
wherein the second delay control block includes:

a direct phase detector for receiving the external clock  
25 signal and a delay modeled internal signal to generate the  
second delay control signal;

a delay model for receiving the second duty controlled

internal clock signal to generate the delay modeled internal signal by delaying the second duty controlled internal clock signal during a predetermined modeled delay time; and

5 a phase mixer for receiving the first internal clock signal, the second internal clock signal, the on-off signal and the weight signal to generate the second duty controlled internal clock signal.

11. The delay locked loop device as recited in claim 5,  
10 wherein the first delay control block includes:

a direct phase detector for receiving the external clock signal and a delay modeled internal signal to generate the first delay control signal;

15 a delay model for receiving the first duty controlled internal clock signal to generate the delay modeled internal signal by delaying the first duty controlled internal clock signal during a predetermined modeled delay time; and

a phase mixer for receiving the first internal clock signal, the second internal clock signal and the weight signal  
20 to generate the second duty controlled internal clock signal.

12. The delay locked loop device as recited in claim 3, wherein the phase detecting block includes:

25 a mixer controller for generating the on-off signal and the weight signal in response to a phase detecting signal; and

a phase detector for generating the phase detecting signal in response to the first internal clock signal and the

second internal clock signal by comparing the phase of the first internal clock signal with the phase of the second internal clock signal.